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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/808,502 | 03/25/2004 | Takehito Tsukamoto | 1186.1033 | 5712 |

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| EXAMINER | |
|---|---|
| NGUYEN, HOA CAO | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2841 | |

DATE MAILED: 05/26/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/808,502 | TSUKAMOTO ET AL. | |
| | Examiner | Art Unit | |
| | Hoa C. Nguyen | 2841 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *12 April 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-51* is/are pending in the application.

4a) Of the above claim(s) *3-20,22,23 and 25-51* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,21 and 24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2 pages*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

1. Claims 3 and 35-51 withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected invention group, there being no allowable generic or linking claim. Within the remaining invention group, claims 1-2 and 4-34, applicants selected Species (a), claims 1-2, 21 and 24, for prosecution. The election was made **without** traverse in the reply filed on 4/12/06. Claims 1-2, 21 and 24 are treated on the merits in this Office Action.

### *Claim Rejections - 35 USC § 102*

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-2 are rejected under 35 U.S.C. 102(b) as being anticipated by Taniguchi et al. (US 6228467).

**Regarding claim 1**, as shown in figures 1a-1c, Taniguchi et al. disclose a multi-layer circuit wiring board (no number) comprising a laminate of films 14/15/16 (film insulator, col.3:24-27), each film having a wiring pattern 2 (electrical conductive pattern, col.3:25) formed on at least one surface thereof, wherein the wiring pattern formed on each film is electrically connected with the wiring pattern formed on another film which is disposed neighboring thereto through a via-contact layer 3 (conductive paste filled in a through-hole, col.3:6-8 and col.3:25-26) formed in any one of the neighboring films.

**Regarding claim 2**, as shown in figures 1a-1c, Taniguchi et al. disclose the films have almost the same thickness (as shown in the figures).

***Claim Rejections - 35 USC § 103***

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

6. Claim 21 is rejected under 35 U.S.C. 103(a) as being unpatentable over Taniguchi et al. (US 6228467) in view of Celaya et al. (US 20020134582).

As shown in figures 1a-1c, Taniguchi et al. disclose a multi-layer circuit wiring board comprising:

(a) A laminate of resin films 14/15/16 (film insulator made of thermal plastic resin, col.3:24-27 and col.4:15-22), each resin film having a wiring pattern 2 (electrical conductive pattern, col.3:25) formed on at least one surface thereof, wherein the wiring pattern formed on one resin film is electrically connected with a wiring pattern 2 (same reference number) formed on another resin film which is disposed next to the one resin

film, through a via-contact layer 3 (conductive paste filled in a through-hole, col.3:6-8 and col.3:25-26) provided on the one resin film or on the another resin film.

But, Taniguchi et al. failed to disclose the wiring pattern 2 formed on an outermost resin film on one side of the laminate is a wiring pattern for mounting an IC, and the wiring pattern 2 formed on another outermost resin film on another side of the laminate is a wiring pattern to be electrically connected with a printed wiring board. However, Taniguchi et al. do disclose the board is for uses in a wide range of circuit board technology (col.1:35-43).

Celaya et al., as shown in figure 1, disclose an interposer 12 (a substrate, also conventionally known as a multilayer wiring board), a circuit pattern 71 (circuit interconnect traces) formed on top surface of the interposer for connecting to IC 20 (semiconductor die), and a circuit pattern 72 (circuit interconnect traces) formed on the bottom surface of the interposer for connecting the interposer to a PCB 30 (a standard PCB), see paragraphs 13-16.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to employ the teachings from Celaya et al. to have the wiring pattern 2 formed on an outermost resin film on one side of the laminate is a wiring pattern for mounting an IC, and the wiring pattern 2 formed on another outermost resin film on another side of the laminate is a wiring pattern to be electrically connected with a printed wiring board in order to place the board of Taniguchi et al. in uses.

7. Claim 24 is rejected under 35 U.S.C. 103(a) as being unpatentable over Taniguchi et al. (US 6228467) in view of Celaya et al. (US 20020134582).

As shown in figures 1a-1c, Taniguchi et al. disclose a multi-layer circuit wiring board comprising:

(a) A first film 15 (film insulator made of thermal plastic resin, col.3:24-27 and col.4:15-22) having a first wiring pattern 2 (electrical conductive pattern, col.3:25) formed on one surface thereof, a second wiring pattern 2 formed on another surface thereof, and a first via-contact layer 3 (conductive paste filled in a through-hole, col.3:6-8 and col.3:25-26) electrically connecting the first wiring pattern with the second wiring pattern;

(b) a second film 14 (film insulator made of thermal plastic resin, col.3:24-27 and col.4:15-22) provided with a third wiring pattern 2 on one surface thereof, another surface thereof being superimposed on the one surface of the first film;

(c) a third film 16 (film insulator made of thermal plastic resin, col.3:24-27 and col.4:15-22) provided on one surface thereof with a fourth wiring pattern, another surface thereof being superimposed on the other surface of the first film;

(d) a second via-contact layer 3 for electrically connecting the first wiring pattern with the third wiring pattern; and

(e) a third via-contact layer 3 for electrically connecting the second wiring pattern with the fourth wiring pattern 2.

However, Taniguchi et al. failed to disclose an IC, a printed wiring board mounting the multi-layer circuit wiring board, the third wiring pattern 2 for mounting an IC, and the fourth wiring pattern to be electrically connected with a printed wiring board.

Celaya et al., as shown in figure 1, disclose an IC package comprising an interposer 12 (a substrate), a circuit pattern 71 (circuit interconnect traces) formed on top surface of the interposer for connecting to IC 20 (semiconductor die), and a circuit pattern 72 (circuit interconnect traces) formed on the bottom surface of the interposer for connecting the interposer to a PCB 30 (a standard PCB), see paragraphs 13-16.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to employ the teachings from Celaya et al. to have the wiring pattern 2 formed on an outermost resin film on one side of the laminate is a wiring pattern for mounting an IC (such as IC 20), and the wiring pattern 2 formed on another outermost resin film on another side of the laminate is a wiring pattern to be electrically connected with a printed wiring board (such as the standard PCB 30) in order to place the board of Taniguchi et al. in uses, and hence providing a complete IC package.

***Citation of Relevant Art***

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

Lijima et al. (US 6351031) disclose a semiconductor device and method for manufacturing substrate of the same.

Bailey et al. (US 6734369) disclose a surface laminar circuit board having pad disposed within a through hole.

Feilchenfeld et al. (US 5798563) disclose a Polytetrafluoroethylene thin film chip carrier.

Maezawa et al. (US 6630630) disclose a multilayer printed wiring board and its manufacturing method.

Okubora et al. (US 6797890) disclose a high frequency module device and method for its preparation.

Ogawa et al. (US 6797367) disclose a multilayer wiring board, semiconductor device mounting board using same, and method of manufacturing multilayer wiring board.

***Conclusion***

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hoa C. Nguyen whose telephone number is 571-272-8293. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kammie Cuneo can be reached on 571-272-1957. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Hoa C. Nguyen
5/18/06

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